Paragraph on page 18, lines 14-23:

Because a write-once memory device cannot re-write over a previously-written location, the temporal mapping technique described above cannot be used with a write-once memory device. Instead, new data is written to a new location. When new data is written, it is preferred that the old data be deleted using the deletion method described above and in U.S. Patent Application Serial No. 09/638,439 (Attorney Docket No. 10519/4) (pending), filed August 14, 2000, to ensure that the file system does not recognize the original data (*e.g.*, pointers) as the current data. To determine the location of the new data, it is preferred that the identifying technique described above be used. This technique will be referred to as spatial mapping (in contrast to temporal mapping) — when data changes at a later time, its location also changes.

IN THE CLAIMS

Please cancel Claims 105, 108, 110, 113, and 125. Also, please amend Claims 104, 106, 107, 109, 111, 112, and 114-120 as follows. Appendix B (at Tab B) contains a marked-up version of those claims showing the changes being made.

104. (Amended) A modular, electronic write-once memory device adapted to be releasably connected to a data storage system, the modular, electronic write-once memory device comprising:

a support element;

error checking and correcting (ECC) code circuitry carried by the support element;

a memory unit carried by the support element and comprising a plurality of write-once memory cells, wherein at least one data bit and at least one ECC bit generated by the ECC code

circuitry based on the at least one data bit are stored in the plurality of write-once memory cells; and

a modular housing protecting the error checking and correcting (ECC) code circuitry and the memory unit.

106. (Amended) The invention of Claim 104, wherein the plurality of write-once memory cells are arranged in a plurality of layers stacked vertically above one another in a single chip.

107. (Amended) The invention of Claim 104, wherein the electronic memory device is selected from the group consisting of a semiconductor-transistor-technology-based memory device, a magnetic-based memory device, and an organic-electronics-based memory device.

109. (Amended) A method for storing data and error checking and correcting (ECC) code bits in a modular, electronic write-once memory device, the method comprising:

providing a modular, electronic write-once memory device adapted to be releasably connected to a data storage system, the modular, electronic write-once memory device comprising a support element, error checking and correcting (ECC) code circuitry carried by the support element, and a memory unit carried by the support element and comprising a plurality of write-once memory cells;

with the modular, electronic write-once memory device, receiving at least one data bit to be stored in the write-once memory cells;

with the ECC code circuitry, generating at least one ECC bit based on the at least one data bit; and

storing the at least one data bit and the at least one ECC bit in the write-once memory cells.

111. (Amended) The invention of Claim 109, wherein the plurality of write-once memory cells are arranged in a plurality of layers stacked vertically above one another in a single chip.

112. (Amended) The invention of Claim 109, wherein the electronic memory device is selected from the group consisting of a semiconductor-transistor-technology-based memory device, a magnetic-based memory device, and an organic-electronics-based memory device.

114. (Amended) A modular three-dimensional electronic memory device adapted to be releasably connected to a data storage system, the modular three-dimensional electronic memory device comprising:

a support element;

error checking and correcting (ECC) code circuitry carried by the support element;

a memory unit carried by the support element and comprising a plurality of memory cells arranged in a plurality of layers stacked vertically above one another in a single chip, wherein at least one data bit and at least one ECC bit generated by the ECC code circuitry based on the at least one data bit are stored in the plurality of memory cells; and

a modular housing protecting the error checking and correcting (ECC) code circuitry and the memory unit.

115. (Amended) The invention of Claim 114, wherein the memory cells comprise write-once memory cells.

116. (Amended) The invention of Claim 114, wherein the modular, electronic memory device is selected from the group consisting of a semiconductor-transistor-technology-based memory device, a magnetic-based memory device, and an organic-electronics-based memory device.

117. (Amended) A method for storing data and error checking and correcting (ECC) code bits in a modular, electronic memory device, the method comprising:

providing a modular, electronic memory device adapted to be releasably connected to a data storage system, the modular, electronic memory device comprising a support element, error checking and correcting (ECC) code circuitry carried by the support element, a memory unit carried by the support element and comprising a plurality of memory cells arranged in a plurality of layers stacked vertically above one another in a single chip, and a modular housing protecting the error checking and correcting (ECC) code circuitry and the memory unit;

with the modular, electronic memory device, receiving at least one data bit to be stored in the memory cells;

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with the ECC code circuitry, generating at least one ECC bit based on the at least one data bit; and

storing the at least one data bit and the at least one ECC bit in the memory cells.

118. (Amended) The invention of Claim 117, wherein the memory cells comprise write-once memory cells.

119. (Amended) The invention of Claim 117, wherein the modular, electronic memory device is selected from the group consisting of a semiconductor-transistor-technology-based memory device, a magnetic-based memory device, and a organic-electronics-based memory device.

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120. (Amended) A system for storing an error checking and correcting (ECC) bit in a three-dimensional memory array of memory cells in a memory device, the system comprising:

a data storage system; and

a modular, electronic memory device adapted to be releasably coupled to the data storage system, the modular, electronic memory device comprising:

a plurality of memory cells arranged in a plurality of layers stacked vertically above one another in a single chip; and

a modular housing protecting the three-dimensional memory array;

wherein the data storage system comprises an error checking and correcting (ECC) code generator and is operative to store at least one data bit and at least one error checking and